IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	Jensen
Application No.	:	10/052,277
Filed	:	01/17/2002
For	:	LOW-POWER BUS INTERFACE

APPEAL BRIEF

On Appeal from Group Art Unit 2112

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VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: ~~05/27/2007~~ 2/26/07

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A system comprising: a plurality of components each having a bus interface, a bus structure that is configured to facilitate communications among the plurality of components, and an activity detector that is configured to detect an initiation of a data-transfer operation and to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of said components, wherein the bus interface is configured to be enabled to receive data from the bus structure as part of said data-transfer operation upon receipt of the enabling signal from the activity detector.

2. The system of claim 1, wherein the activity detector is further configured to detect a completion of the data-transfer operation, and terminates the enabling signal based on the completion of the data-transfer operation, and the bus interface is configured to be disabled from receiving data from the bus structure upon termination of the enabling signal.

3. The system of claim 1, wherein the enabling signal includes a gated clock signal.

4. The system of claim 1, wherein the bus interface includes a plurality of clocked deivces that are clocked based on the enabling signal.

5. The system of claim 1, wherein the activity detector includes: a set-reset device that is set upon detection of the initiation of the data-transfer operation, and a delay device,

operably coupled to the set-reset device, that is configured to provide the enabling signal synchronous with a system clock that is common to the bus structure, based on whether the set-reset device is set.

6. The system of claim 5, wherein the set-reset device is reset upon detection of a completion of the data-transfer operation.

7. The system of claim 1, further including a bus controller that is configured to establish a communications path between an initiating component of the plurality of components and a target component of the plurality of components, wherein the activity detector provides the enabling signal within a time duration consumed by the bus controller to establish the communications path.

8. The system of claim 7, wherein the bus controller includes one or more devices that operate in dependence upon the enabling signal.

9. (Canceled)

10. A method of reducing power consumption in a system comprising a plurality of components each having a bus interface that are configured to communicate via a bus structure, comprising: detecting an initiation of a data transfer operation by a component of the plurality of components, communicating an enabling signal to more than one other components of the plurality of components, and enabling a bus interface at each of the

more than one other components to receive data signals as part of the data transfer operation, based on the enabling signal.

11. The method of claim 10, further including detecting a completion of the bus activity, and disabling the bus interface at each of more than one other components, based on the completion of the bus activity.

12. The method of claim 10, further including synchronizing the enabling signal to a system clock that is common to the bus structure.

13. The method of claim 10, further including establishing a communications path between the component that initiated the bus activity and a target component of the more than one other components, and enabling the bus interface at the target component within a time duration required to establish the communications path.

14. (Canceled)

15. An electronic circuit comprising: a plurality of initiators that are configured to selectively initiate data-transfer operations via a bus structure, an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to generate therefrom an enabling signal, and a plurality of targets that are configured to process the data-transfer operations, each of the plurality of targets including an interface for receiving the data-transfer operations, wherein the interface of

each of the plurality of targets is configured to receive data of the data-transfer operations in dependence upon the enabling signal from the activity detector.

16. The electronic circuit of claim 15, wherein the plurality of initiators are configured to effect the data-transfer operations at a system clock speed, and the interface of each of the plurality of targets is configured to operate at the system clock speed only when the activity detector provides the enabling signal.

17. The electronic circuit of claim 16, wherein the enabling signal includes a clocking signal that operates at the system clock speed.

18. The electronic circuit of claim 15, wherein the activity detector is further configured to detect the completion of the data-transfer operations, and to terminate the generation of the enabling signal based on a completion of the data-transfer operations.

19. The electronic circuit of claim 15, further including a bus controller that is configured to establish a communications path between an initiator of the plurality of initiators and a target of the plurality of targets, wherein the activity detector is configured to generate the enabling signal within a time duration required by the bus controller to establish the communications path.